REMARKS

The Examiner has rejected Claims 1-12 under 35 U.S.C. 103(a) as being unpatentable over Dai et al. (U.S. Patent No. 6,246,692), in view of Christensen et al. (U.S. Patent No. 5,491,687). Applicant respectfully disagrees with such rejection, especially in view of the amendments made hereinabove to the independent claims. Specifically, applicant has amended the independent claims to at least substantially include the subject matter of former dependent Claim 9.

With respect to independent Claim 1, the Examiner has relied on the following excerpt from Dai to make a prior art showing of applicant's claimed technique "wherein a link aggregation port is selectively aggregated to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules."

> "In the described embodiment, the total bandwidth available in transmitting data and data ring messages to the data ring segment 18 from output 132 of the data ring transmit and upload control unit 126 is 2.112 Gbps. Therefore, this path may support up to twenty 100 Mbps channels. Data messages are transmitted from output 132 of unit 126 in bursts of 64 bytes (or 512 bits) per second. For a data channel operating at 100 Mbps; one bit is transmitted in 10 nanoseconds, and one burst is transmitted in 5120 nanoseconds. For this embodiment, the period of the channel rate timer may be 5120 nanoseconds. It will be readily understood to those skilled in the art that the bandwidth resource manager 90 may be implemented in accordance with a wide variety of methods. In the described embodiment, the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and..." (Col. 11, lines 27-44 - emphasis added)

Applicant respectfully asserts that the excerpt relied upon by the Examiner merely teaches that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; [and] increased by 10 upon releasing a 100 Mbps channel" (emphasis added). However, simply teaching that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel;

decreased by 1 upon allocating 10 Mbps for a channel; [and] increased by 10 upon releasing a 100 Mbps channel," as in Dai, fails to even suggest "a link aggregation port [that] is selectively aggregated to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules" (emphasis added), as claimed by applicant. Clearly, disclosing that "a bandwidth counter...is...increased by 1 upon releasing a 10 Mbps channel...[and] decreased by 1 upon allocating 10 Mbps for a channel" (emphasis added), as in Dai, fails to even suggest "dynamically set[ting] one or more switch modules' external terminals to selectively aggregate information to and from the switch modules" (emphasis added), as claimed by applicant.

With respect to independent Claim 8, the Examiner has relied on Col. 11, lines 27-55 and Figure 2A from Dai to make a prior art showing of applicant's claimed "selectively activating a link aggregation port to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules."

Applicant respectfully asserts that the excerpt relied upon by the Examiner merely teaches that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased by 10 upon allocating 100 Mbps for a channel" (Col. 11, lines 40-45 - emphasis added). However, simply teaching that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased by 10 upon allocating 100 Mbps for a channel," as in Dai, fails to even suggest "selectively activating a link aggregation port to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules" (emphasis added), as claimed by applicant. Clearly, disclosing that "a bandwidth counter...is...increased by 1 upon releasing a 10 Mbps channel...[and] decreased by 1 upon allocating 10 Mbps for a channel" (emphasis

added), as in Dai, fails to even suggest "dynamically set[ting] one or more switch modules' external terminals to selectively aggregate information to and from the switch modules" (emphasis added), as claimed by applicant.

Further, Figure 2A from Dai merely "shows a detailed schematic circuit block diagram of components of one of the cut-through packet transfer switching devices 12 of the packet switching fabric of 10 (FIG. 1)" (Col. 6, lines 19-22), with "eight transmit buffer queues 144 each having an input 145 connected to receive data from a corresponding one of the eight outputs 143 of the data distribution control unit 140, and an output 146 connected to a corresponding one of eight network output ports 147 designated (A_0, A_1, . . . , A_7)" (Col. 7, lines 12-17). However, simply disclosing "an output...connected to a corresponding one of eight network output ports," as in Dai, fails to even suggest "selectively activating a link aggregation port to respond to the link signal and to dynamically set one or more switch modules' external terminals to selectively aggregate information to and from the switch modules" (emphasis added), as claimed by applicant.

Additionally, with respect to the independent claims, the Examiner has relied on Col. 10, lines 8-67 and Col. 11, lines 27-44 from Dai; Figure 1 and Col. 4, lines 21-40 from Christensen to make a prior art showing of applicant's claimed technique "wherein the statistics are evaluated to generate a link signal representative of desired links/ports to be aggregated" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully asserts that the excerpts from Dai relied upon by the Examiner merely teach that "[a]fter the CRMT processing unit 100 selects an interconnect transaction corresponding to a particular SRC_REQ message, the termination processing unit 100 transfers a GET_RES message to the control ring via transmitting unit 80 to reserve the necessary bandwidth resources for the corresponding interconnect transaction via a source-destination channel" and "[t]he source-destination channel is set up to accommodate the bandwidth of the destination output port" (Col. 10,

lines 59-67 – emphasis added). Furthermore, in Col. 11, lines 40-44, Dai merely teaches "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; [and] increased by 10 upon releasing a 100 Mbps channel" (emphasis added).

However, simply teaching that "the termination processing unit 100 transfers a GET_RES message to the control ring via transmitting unit 80 to reserve the necessary bandwidth resources for the corresponding interconnect transaction via a source-destination channel" and "[t]he source-destination channel is set up to accommodate the bandwidth of the destination output port" (emphasis added), as in Dai, fails to even suggest "the statistics are evaluated to generate a link signal representative of desired links/ports to be aggregated" (emphasis added), as claimed by applicant.

Additionally, simply teaching that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; [and] increased by 10 upon releasing a 100 Mbps channel" (emphasis added), as in Dai, fails to even suggest "the statistics are evaluated to generate a link signal representative of desired links/ports to be aggregated" (emphasis added), as claimed by applicant.

Still yet, applicant respectfully asserts that the excerpt from Christensen relied upon by the Examiner merely teaches that "port 74 maintains current port statistics including the number of good and bad frames passing through port 74, and the operational status of port 74" (Col. 4, lines 22-25 – emphasis added). However, simply disclosing that "port 74 maintains current port statistics including the number of good and bad frames passing through port 74, and the operational status of port 74" (emphasis added), as in Christensen, fails to even suggest "the statistics are evaluated to generate a link signal representative of desired links/ports to be aggregated" (emphasis added), as claimed by applicant.

Furthermore, Figure 1 from Christensen merely shows "a high-level block diagram of a communications network system which includes a LAN switch" (Col. 3, lines 33-34). However, simply disclosing "a communications network system which includes a LAN switch," as in Christensen, fails to even suggest "statistics [that] are evaluated to generate a link signal representative of desired links/ports to be aggregated" (emphasis added), as claimed by applicant.

To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. *In re Vaeck,* 947 F.2d 488, 20 USPQ2d 1438 (Fed.Cir.1991).

Applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the excerpts from the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above. Nevertheless, despite such paramount deficiencies and in the spirit of expediting the prosecution of the present application, applicant has incorporated the subject matter of former Claim 9 into the independent claims.

With respect to the subject matter of former Claim 9 (now at least substantially incorporated into the independent claims), the Examiner has relied on Col. 7, lines 31-44 and Col. 11, lines 27-55 from Dai to make a prior art showing of applicant's claimed "selectively introducing marker information into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified" (see this or similar, but not necessarily identical language in the independent claims).

Applicant respectfully asserts that the excerpts relied upon by the Examiner merely teach that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased by 10 upon allocating 100 Mbps for a channel" (Col. 11, lines 40-45 - emphasis added).

However, simply teaching that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased by 10 upon allocating 100 Mbps for a channel," as in Dai, fails to even suggest "selectively introducing **marker information** into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified" (emphasis added), as claimed by applicant.

Furthermore, in Col. 7, lines 39-44, Dai discloses "a control port 171 connected to receive queuing control signals from the packet buffer memory control port 157 of the input queuing control unit 152 and also providing data address pointer information to control port 157 of the input queuing control unit" (emphasis added). However, simply disclosing "a control port 171...providing **data address pointer information** to control port 157 of the input queuing control unit" (emphasis added), as in Dai, fails to even suggest "selectively introducing **marker information** into the data to ensure that the integrity of the data is reasonably maintained when a link aggregation is modified" (emphasis added), as claimed by applicant.

Applicant further notes that the prior art is also deficient with respect to the dependent claims. For example, with respect to Claim 7, the Examiner has relied on Col. 7, lines 31-44 and Col. 11, lines 27-55 from Dai to make a prior art showing of applicant's claimed technique "wherein...the master management processor is configured to introduce the marker information into the data to ensure that the integrity of the data is reasonably maintained when the link aggregation is modified."

Applicant respectfully asserts that the excerpt relied upon by the Examiner merely teaches that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased by 10 upon allocating 100 Mbps for a channel" (Col. 11, lines 40-45 - emphasis added). However, simply teaching that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased by 10 upon allocating 100 Mbps for a channel," as in Dai, fails to even suggest that "the master management processor is configured to introduce the marker information into the data to ensure that the integrity of the data is reasonably maintained when the link aggregation is modified" (emphasis added), as claimed by applicant.

Furthermore, in Col. 7, lines 39-44, Dai discloses "a control port 171 connected to receive queuing control signals from the packet buffer memory control port 157 of the input queuing control unit 152 and also providing data address pointer information to control port 157 of the input queuing control unit" (emphasis added). However, simply disclosing "a control port 171...providing data address pointer information to control port 157 of the input queuing control unit" (emphasis added), as in Dai, fails to even suggest that "the master management processor is configured to introduce the marker information into the data to ensure that the integrity of the data is reasonably maintained when the link aggregation is modified" (emphasis added), as claimed by applicant.

Additionally, with respect to Claim 11, the Examiner has relied on Col. 11, lines 27-55 from Dai to make a prior art showing of applicant's claimed "sending a marker to facilitate handover from a first port to a second port."

Applicant respectfully asserts that the excerpt relied upon by the Examiner merely teaches that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased

by 10 upon allocating 100 Mbps for a channel" (Col. 11, lines 40-45 - emphasis added). However, simply teaching that "the bandwidth resource manager 90 has a bandwidth counter which is: increased by 1 upon releasing a 10 Mbps channel; decreased by 1 upon allocating 10 Mbps for a channel; increased by 10 upon releasing a 100 Mbps channel; and decreased by 10 upon allocating 100 Mbps for a channel," as in Dai, fails to even suggest "sending a marker to facilitate handover from a first port to a second port" (emphasis added), as claimed by applicant.

Again, applicant respectfully asserts that at least the third element of the *prima facie* case of obviousness has not been met, since the prior art references, as relied upon by the Examiner, fail to teach or suggest all of the claim limitations, as noted above.

Thus, a notice of allowance or specific prior art showing of each of the foregoing claim elements, in combination with the remaining claimed features, is respectfully requested.

Still yet, applicant brings to the Examiner's attention the subject matter of new Claims 13-14 below, which are added for full consideration:

> "wherein the statistics are used for load-balancing purposes" (see Claim 13); and
>
> "wherein a marker technique is employed to prevent an out-of-order problem when handing over traffic from the first port to the second port" (see Claim 14).

Again, a notice of allowance or a proper prior art showing of all of applicant's claim limitations, in combination with the remaining claim elements, is respectfully requested.

Thus, all of the independent claims are deemed allowable. Moreover, the remaining dependent claims are further deemed allowable, in view of their dependence on such independent claims.

In the event a telephone conversation would expedite the prosecution of this application, the Examiner may reach the undersigned at (408) 505-5100. The Commissioner is authorized to charge any additional fees or credit any overpayment to Deposit Account No. 50-1351 (Order No. RMI1P013).

Respectfully submitted,
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